Circuit Emulation over IP/MPLS

BRKBBA-3012

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Cisco Networkers 2007

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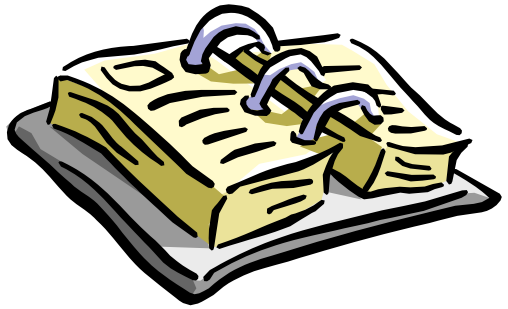
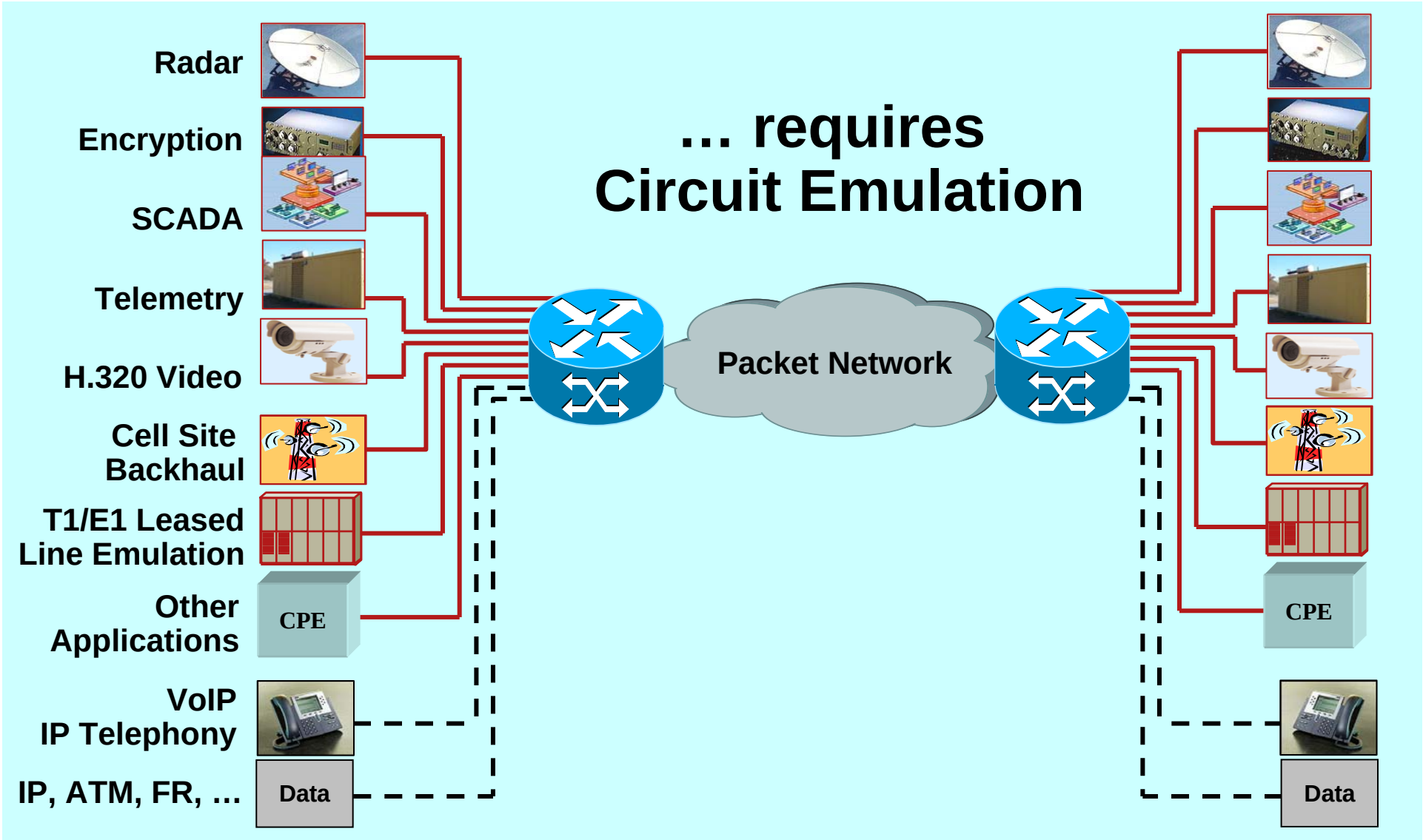
Agenda



- Background
- Circuit Emulation over IP/MPLS Encapsulation
- Control Plane
- Clocking
- Hardware
- Standards

Circuit Emulation
Background

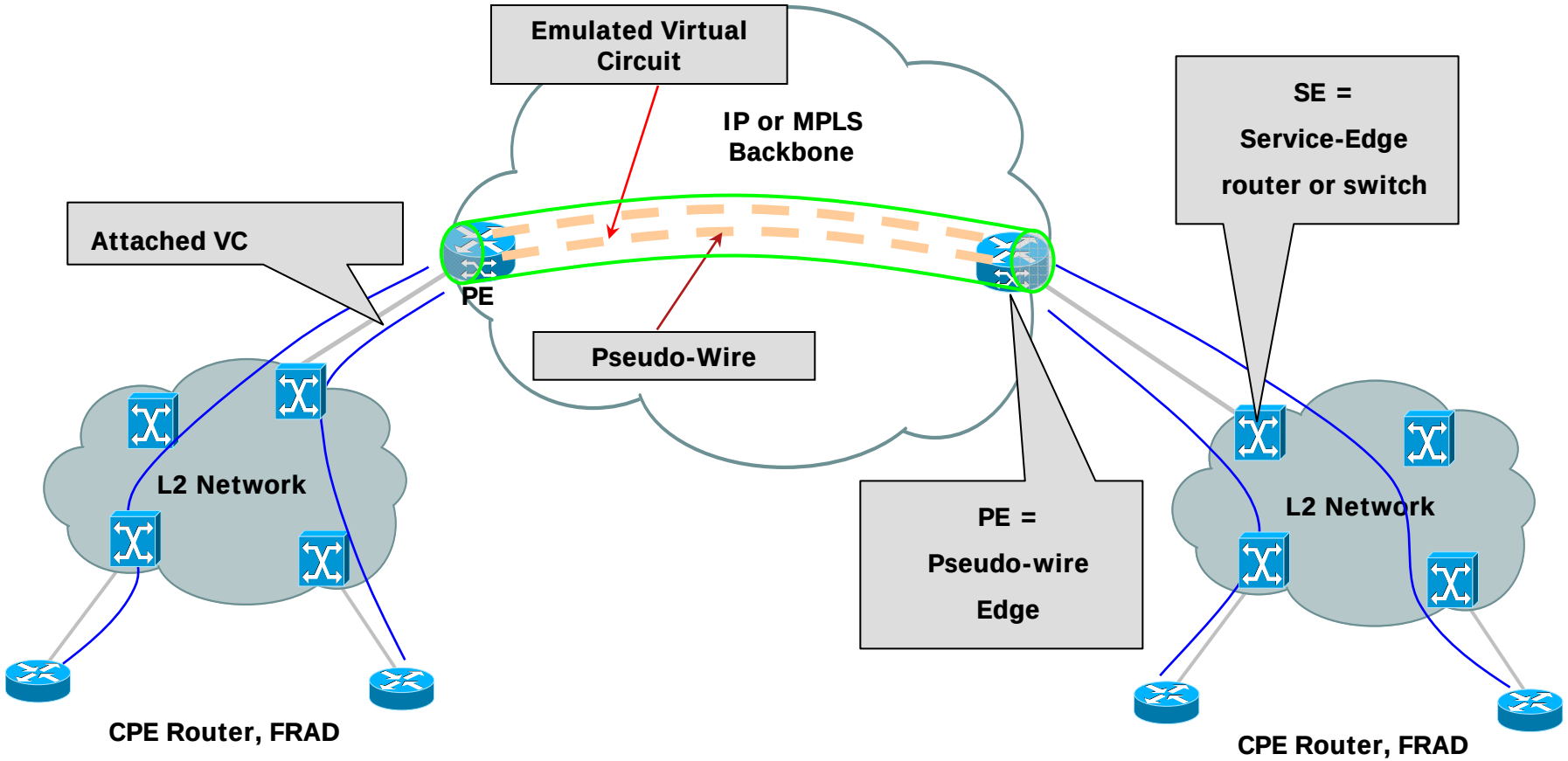
IP NGN is about having 1 network for all services



Pseudowires

- One purpose of PWs is to support the convergence of networks to an IP/MPLS core by carrying traditional “transport” mechanisms over IP/MPLS.
- The first wave of widely deployed PWs were concerned with the emulation of data-services: Frame-relay, Ethernet, ATM, HDLC.
- The second wave of deployments is concerned with the development of more complex PW hierarchies (Multi Segment-PWs) and with the emulation of synchronous transport mechanisms such as TDM, SONET/SDH and associated with a clocking model.
- This talks focuses on some of the emulation of synchronous transport mechanisms.

IETF : Circuit Emulation (Pseudo-Wire Emulation Edge to Edge)

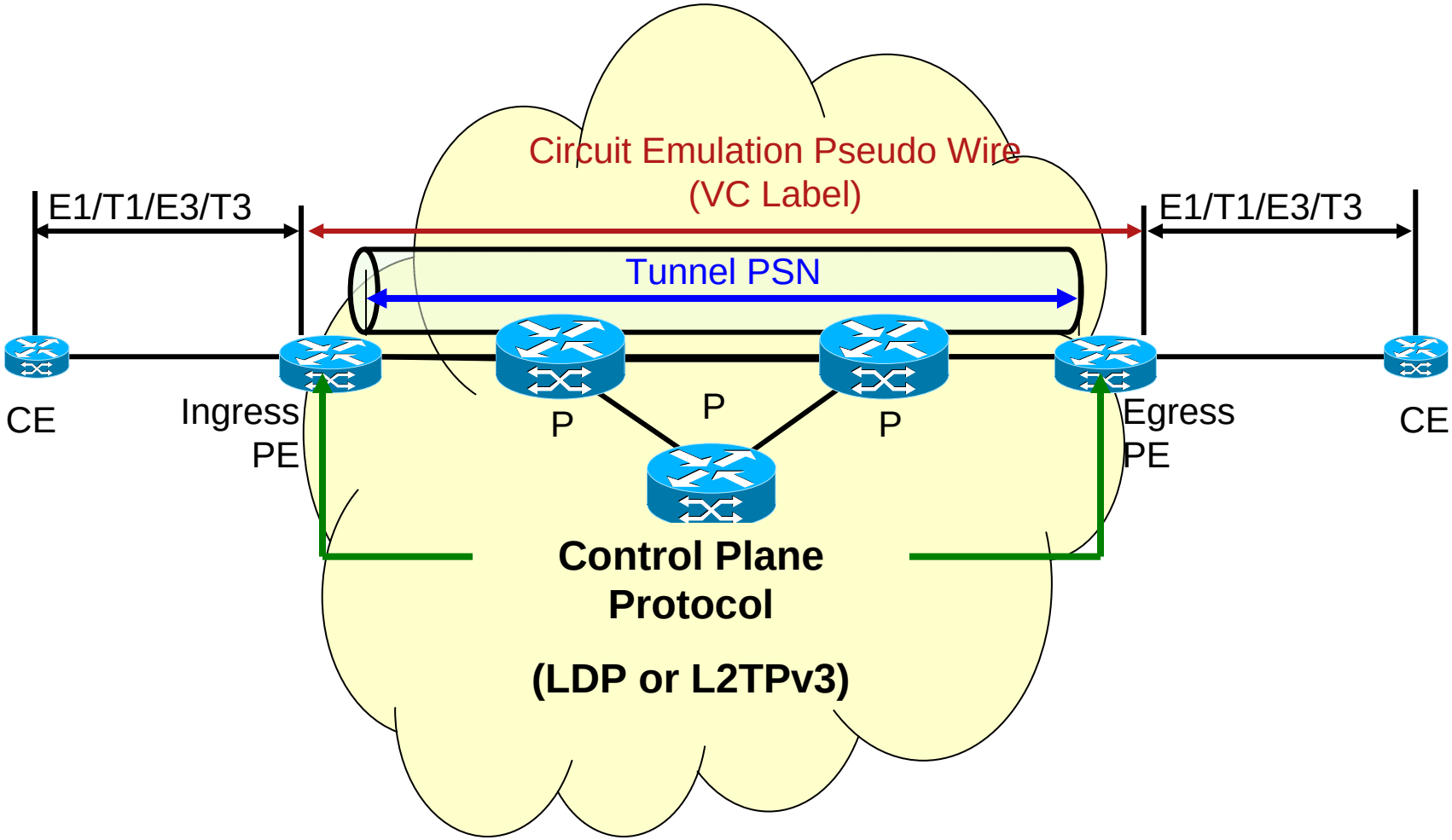


Circuit Emulation over IP/UDP (no control plane)

Circuit Emulation over IP = TDM extension for L2TPv3

Circuit Emulation over MPLS = TDM extension for LDP-CP

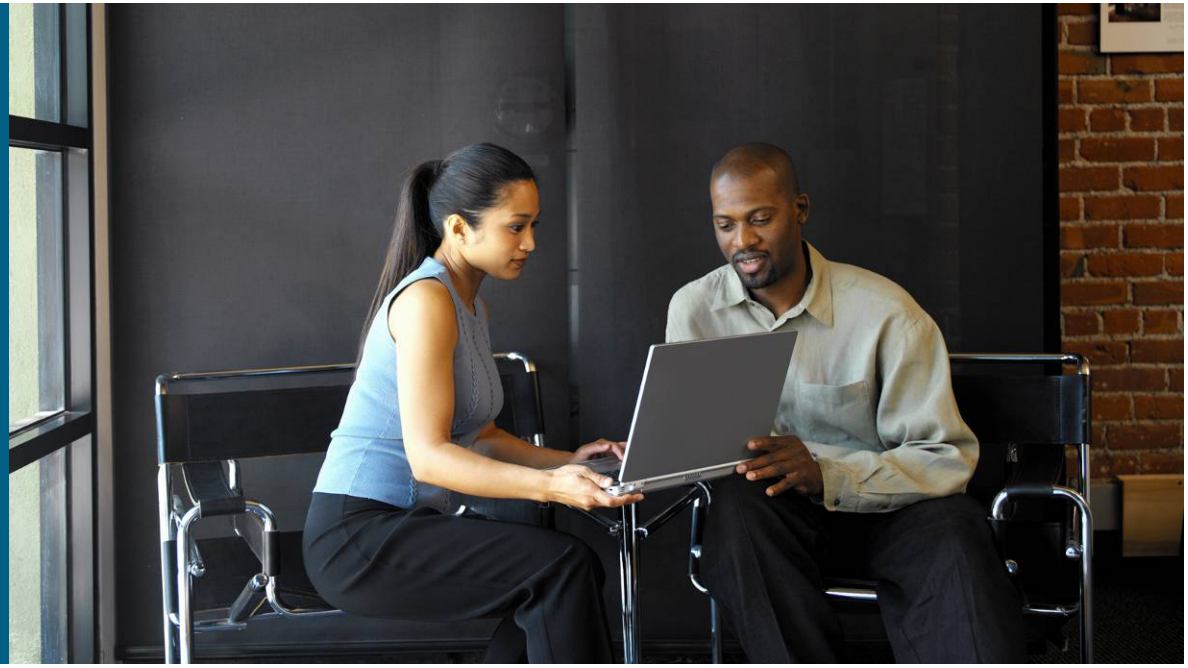
Circuit Emulation semantic



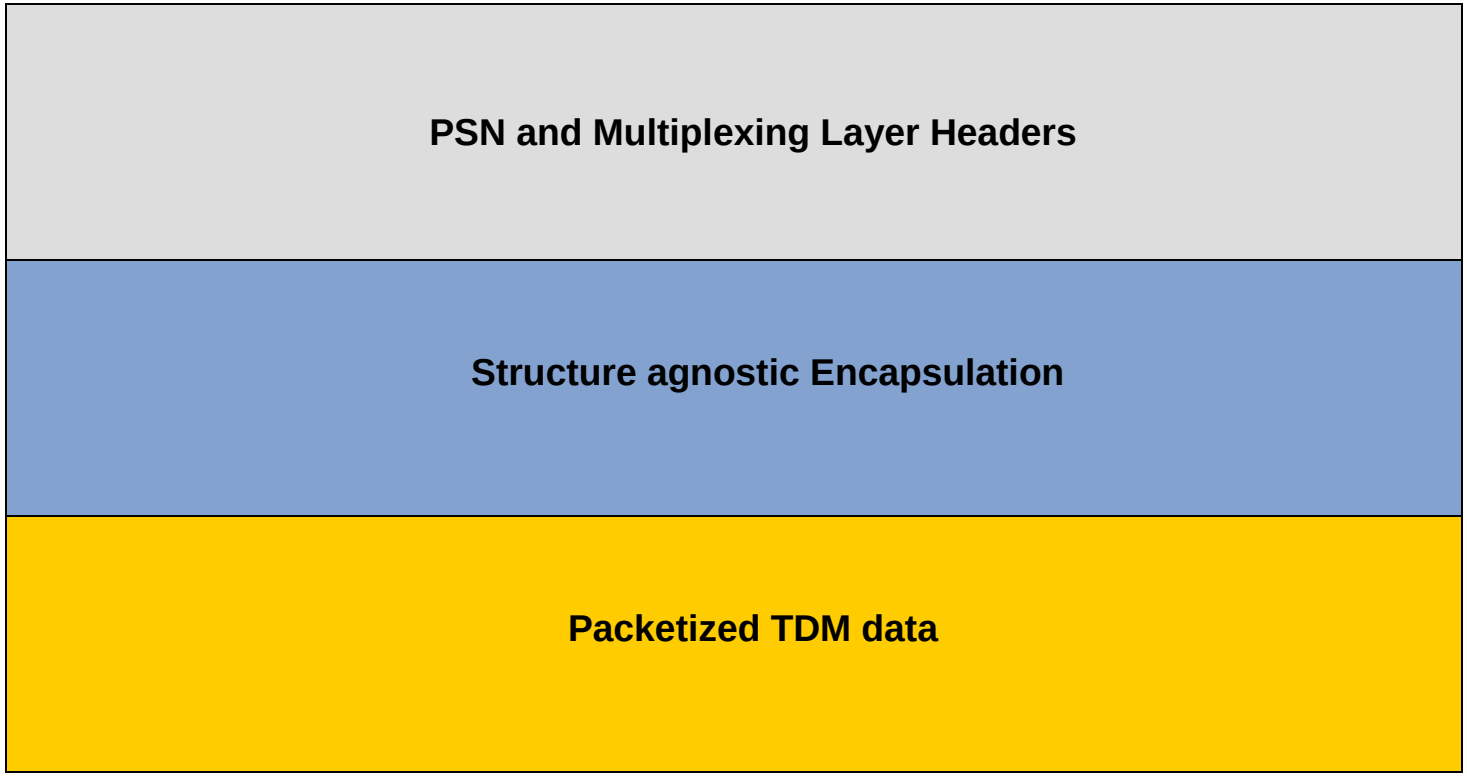
Standards Taxonomy

- There are a number of standards bodies working on the transport of synchronous services: IETF, ITU, MEF, MFA
- The encapsulation and control work at these standards bodies has been well co-ordinated. The structure and language is different, but the underlying technology is identical.
- Most of the control plane work is being done in the IETF
- There are two classes of synchronous circuit emulations:
  - TDM (T1/E1 up to T3/E3)
  - SDH/SONET (not covered in this presentation)
- There are three methods of carrying TDM over IP/MPLS:
  - Structure Agnostic (SAToP)
  - Structure Locking (CESoPSN)
  - Structure Indication/Recovery (TDMoIP)
- There are three implementation supported:
  - IP / UDP
  - IP / L2TPv3
  - MPLS

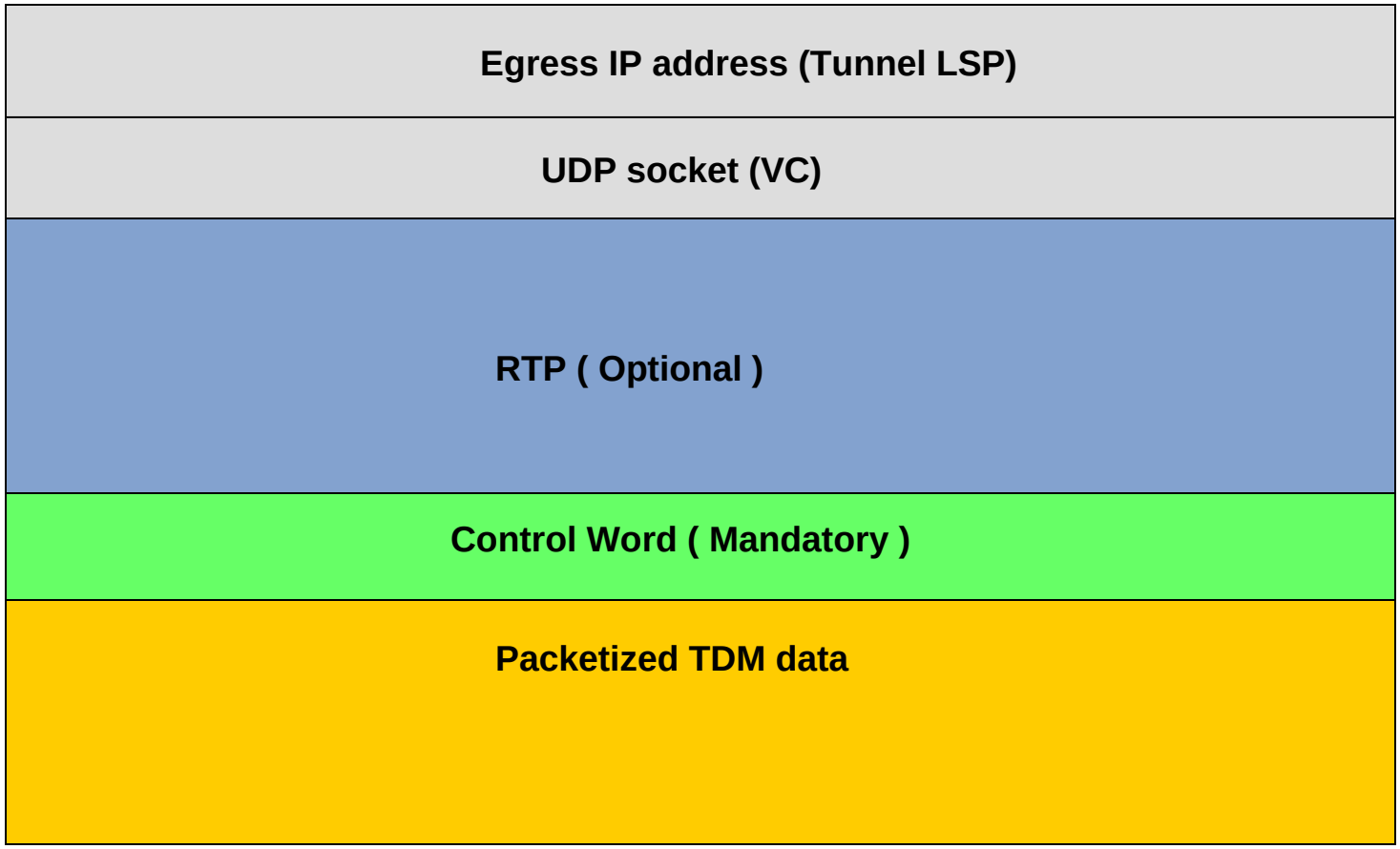
Circuit Emulation
Structure Agnostic



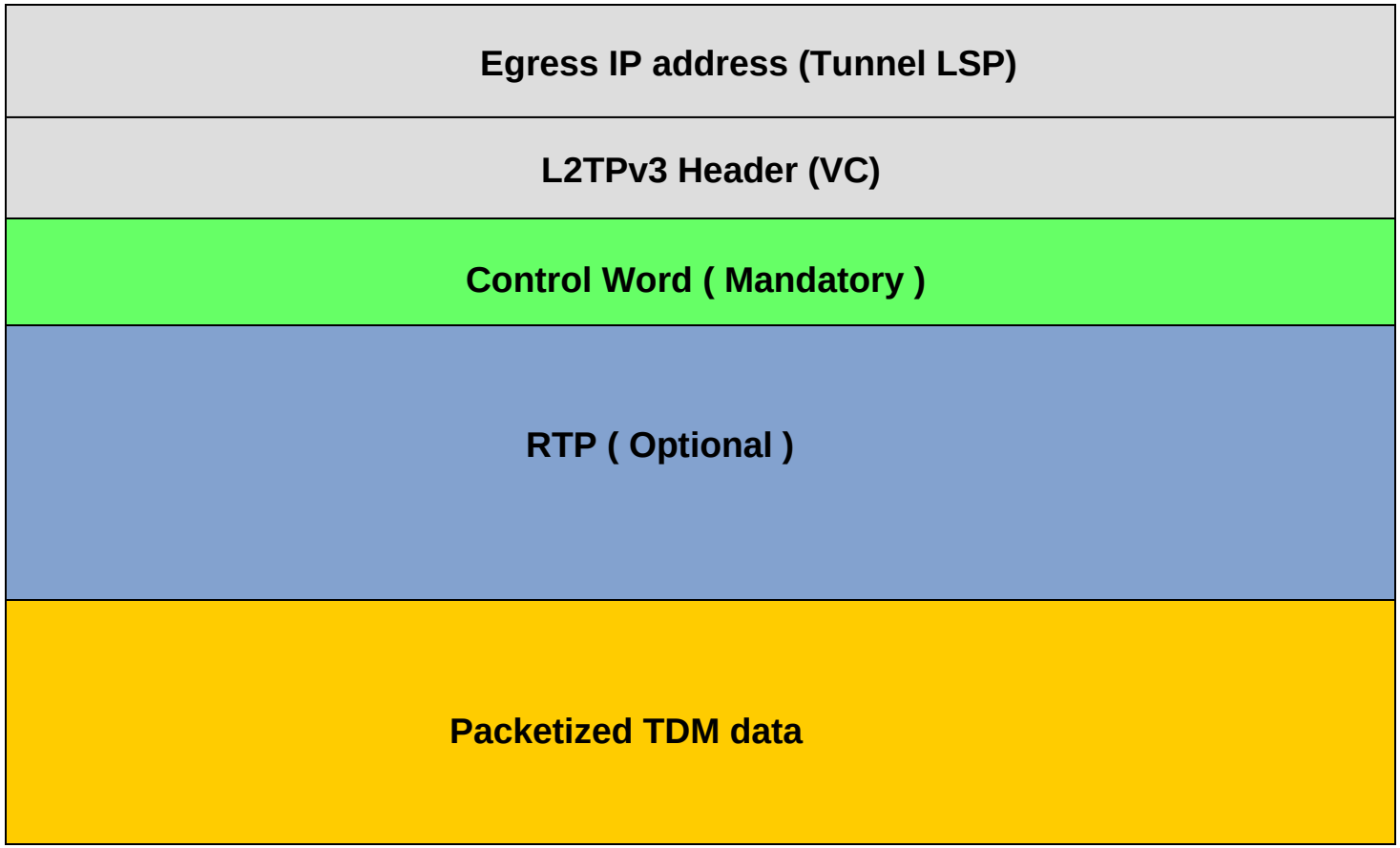
Basic structure agnostic Packet Format



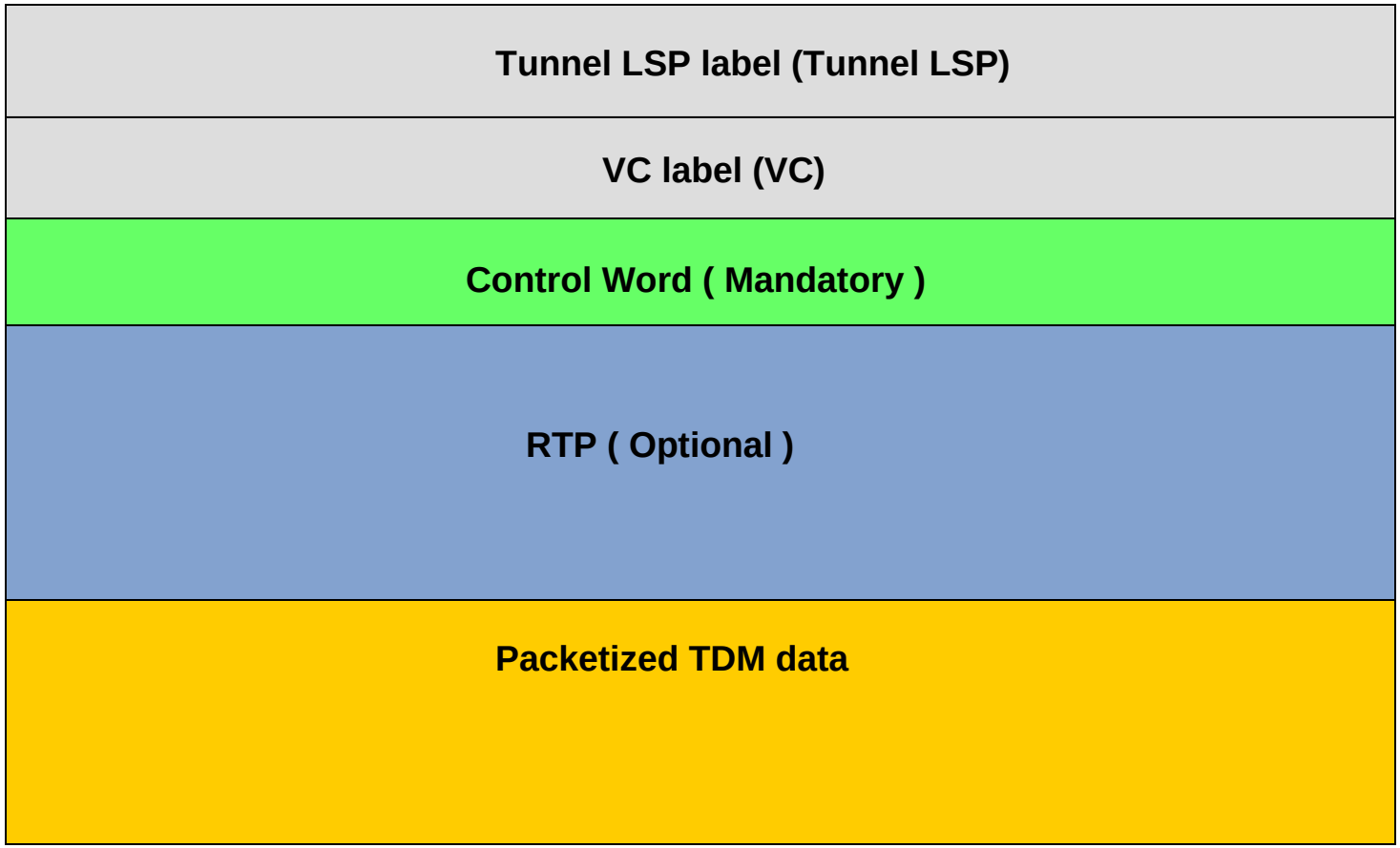
UDP (no control plane)



L2TPv3 (L2TPv3 control plane)

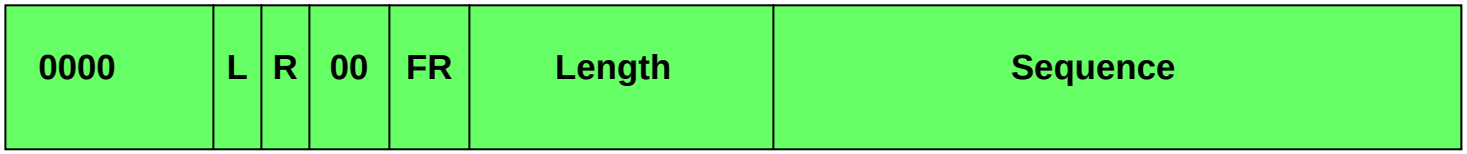


MPLS (LDP control plane or static)



Structure agnostic : Control Word

The CW is used to signal per packet control information

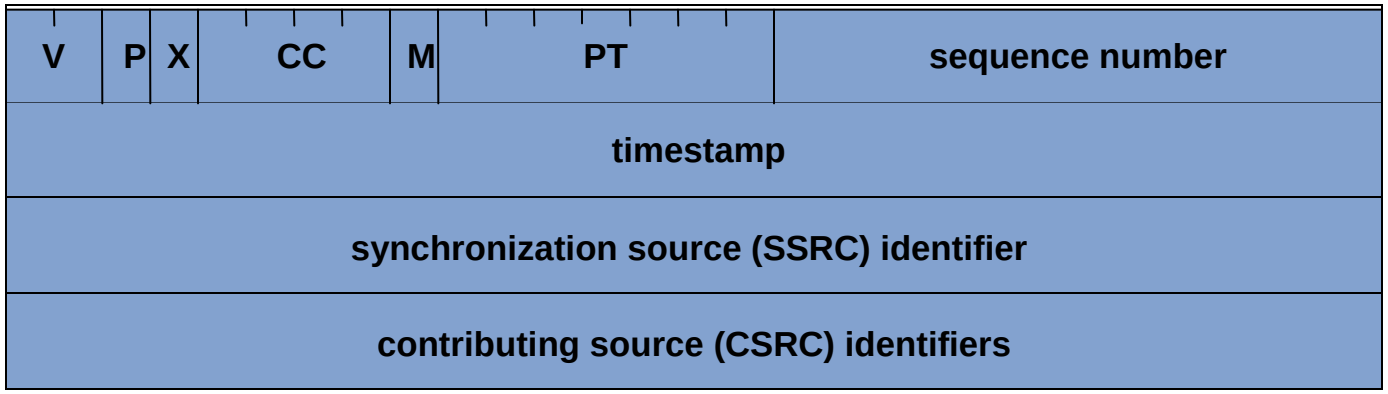


0-3	**0000**	Reserved
4	**L**	Payload invalid due to attachement circuit fault
5	**R**	if set, indicates that local CE-bound interface is in the packet loss state.
6-7	**00**	Reserved
8-9	**FR**	defined in draft [PWE3-fragmentation]: not used except for CAS packets
10-15	**Length**	CEM Header + Payload
16-31	**Sequence**	16 bit unsigned SN includes 0 [RFC3550]

RTP Header

- RTP Header is optional
- RTP Header is used when using separate clock sources for adaptive clock mechanism.
- Equivalent to ATM Circuit Emulation SRTS (Synchronous Residual Time Stamp).

RTP header (fixed)



- **version (v): 02**
- **padding (p): 0**
- **extension (x): 0**
- **CSRC count (CC): 0**
- **marker (M): 0**
- **payload type (PT):** Selected from the dynamic range. MAY be identical for both ends. Used to verify config.
- **sequence number:** The Sequence Number is identical to the Sequence Number in the CW.
- **timestamp:** the timestamp reflects the sampling instant of the first octet in the RTP data packet. May be used in absolute or relative mode.
- **SSRC:** used to identify misconfigurations

Structure agnostic Payload

- Bytes taken sequentially from AC and put into payload
- No attempt is made to locate any structure in payload
- The following payload sizes MUST be supported
  - –E1 256 bytes TDM data payload
  - –T1 192 bytes TDM data payload
  - –E3/T3 1024 bytes TDM data payload
- There is also an octet aligned mode used in conjunction with SONET/SDH that carries data units of 200 bytes (i.e. units of payload 1ms long)

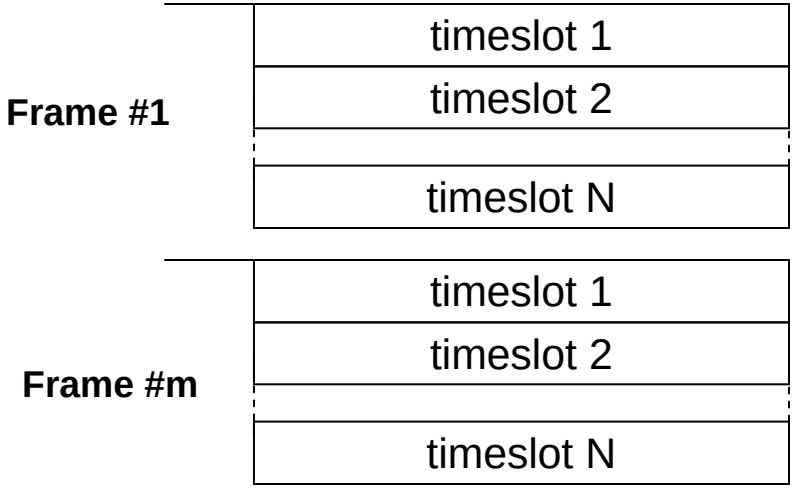
Circuit Emulation
Structure locking

Packet Format

- The payload format is unique to structure locking
- The CW signals some additional states
- All other aspects of the prototol are identical to structure agnostic.

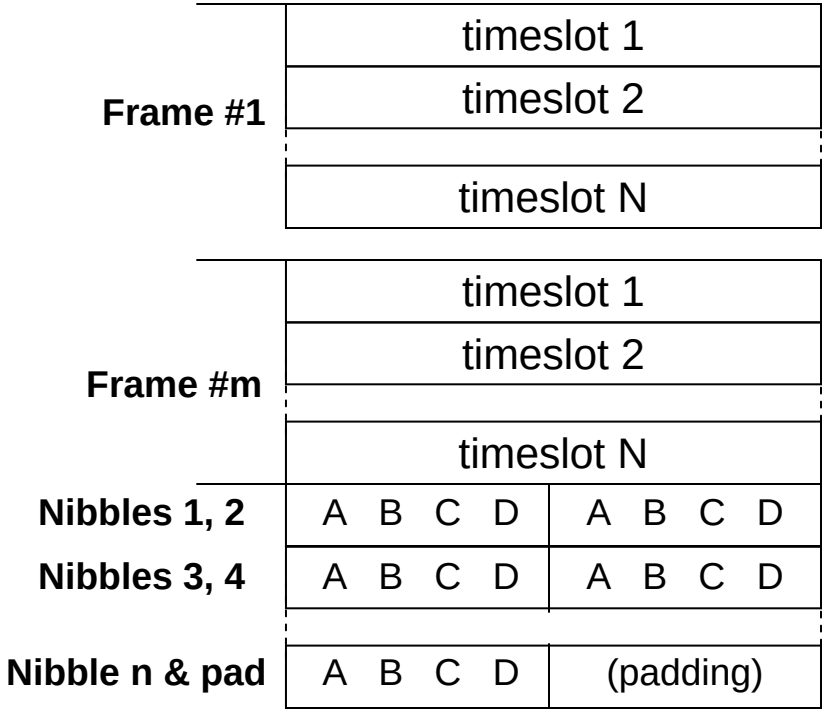
Payload structure locking basic

- Payload is NxDS0
- If N=1 then DS0 payload size = 64 bytes
- If N=2, 3 or 4 DS0 payload size = 32 bytes
- If N>4 DS0 payload size = 8 bytes



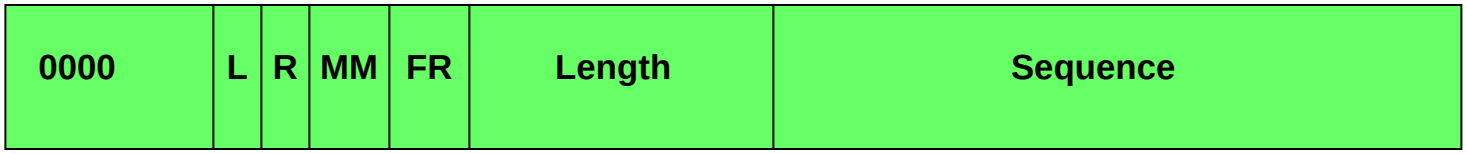
Payload structure locking with CAS (in-band) (Communicating Applications Specifications)

- CAS nibbles are added at end of Frames Sequences



Control Word

As for structure agnostic Except as shown



4	L	if set, indicates some abnormal condition of AC
6-7	MM [CESoPSN]	if L is cleared then MM indicates 00 structure locking data packet is in normal condition 10 structure locking data packet, RDI condition of the AC 11 structure locking signaling packet (CAS) if L is set then MM indicated 00 TDM data invalid
8-9	FR	defined in draft [PWE3-fragmentation]: not used except for trunk specific NxDS0 with CAS, in which as they may be used to indicate fragmentation of multiframe packets.

Circuit Emulation

Structure

Indication/Recovery

Structure Indication/Recovery Packet Format

- The payload format is unique to structure indication/recovery and consists of ATM AAL1 & AAL2 PDUs. Note this is the 48 byte ATM payload, NOT the 53 byte ATM cell.
- Chosen so that the TDM over ATM designs could be reused.
- AAL1 used for fixed rate
- AAL2 used for variable rate, including silence suppression
- The CW signals some additional states
- All other aspects of the protocol are identical to SAToP

Control Word

As for structure agnostic Except as shown

4	L	if set, indicates some abnormal condition of AC
6-7	MM	if L is cleared then MM indicated 00 TDMoIP data packet is in normal condition If L is set 00 TDM defect that should trigger conditioning or AIS gen 01 TDM idle, do not trigger alarm, if config send idle 10 corrupted, potentially recoverable, data

AAL Payload Format

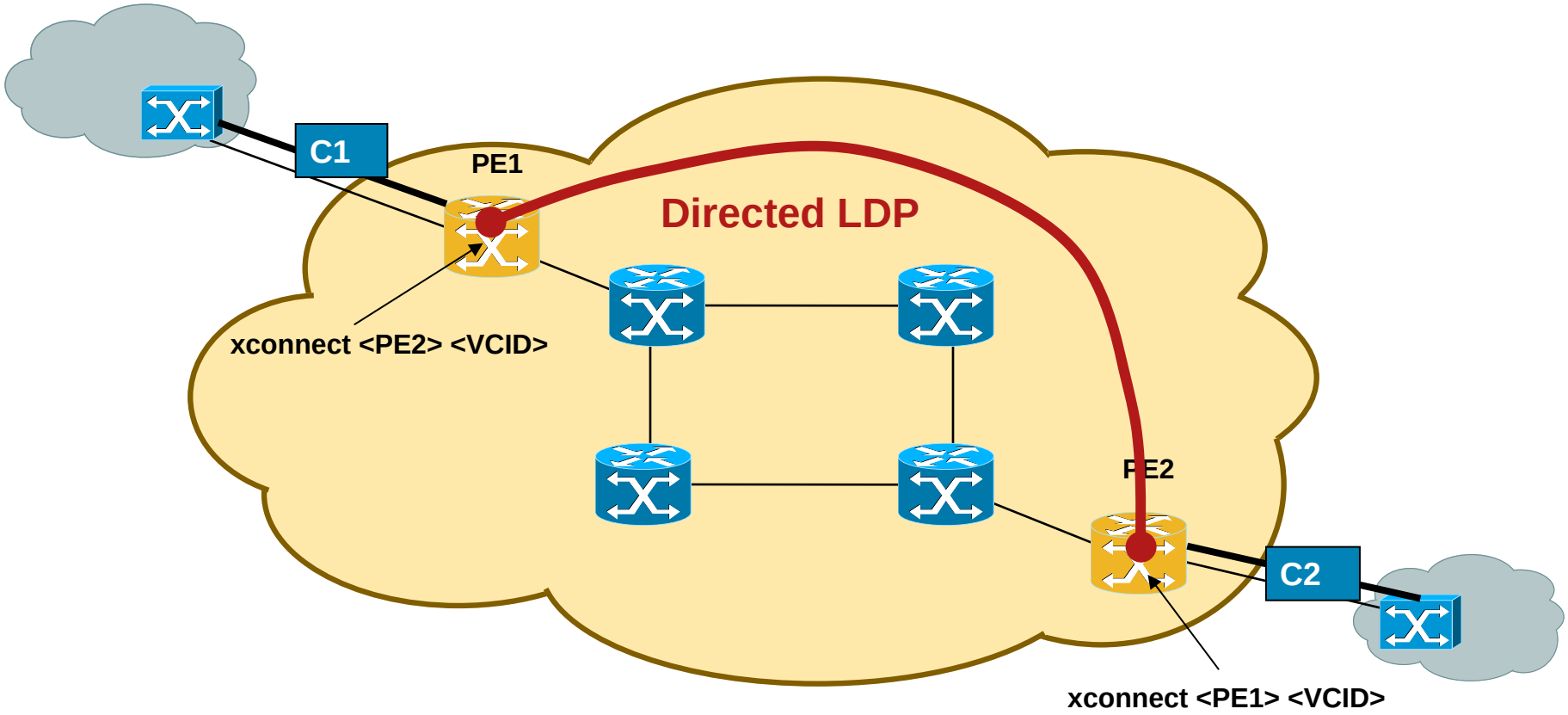
- AAL1 – Unstructured – one byte of overhead + 47 bytes of payload per PDU
- AAL1 – Pointer format - one byte of overhead + one byte of pointer every other PDU + 46/47 bytes of data
- AAL2 – 3 bytes overhead per PDU

Circuit Emulation
Control Plane

Methods to distribute VC Labels

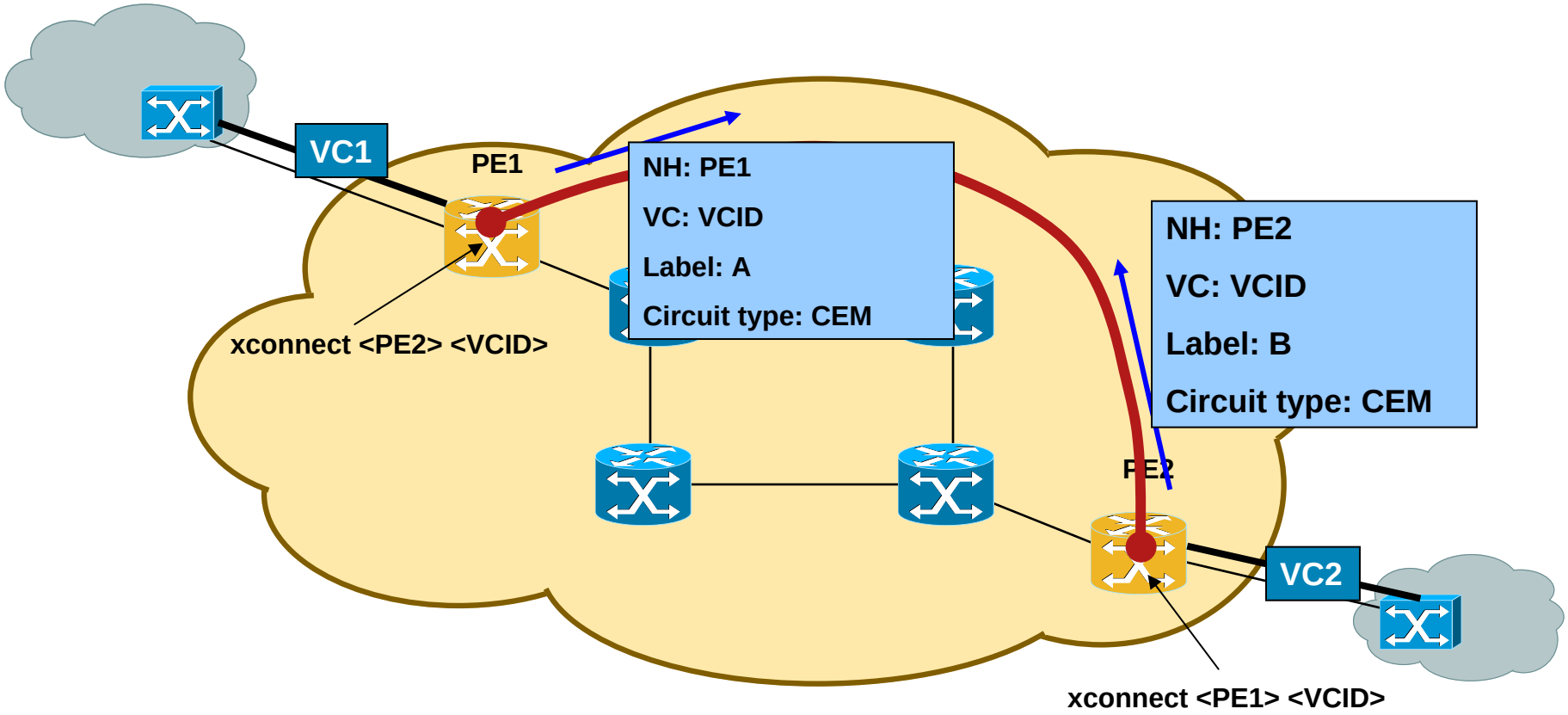
- Static UDP port
- L2TPv3
- Static assigned label
- LDP with PWid FEC TLV
- LDP with Generalized FEC TLV

AToM: PWid FEC signaling



Based on xconnect command, both PE's will create directed LDP session if doesn't exist already

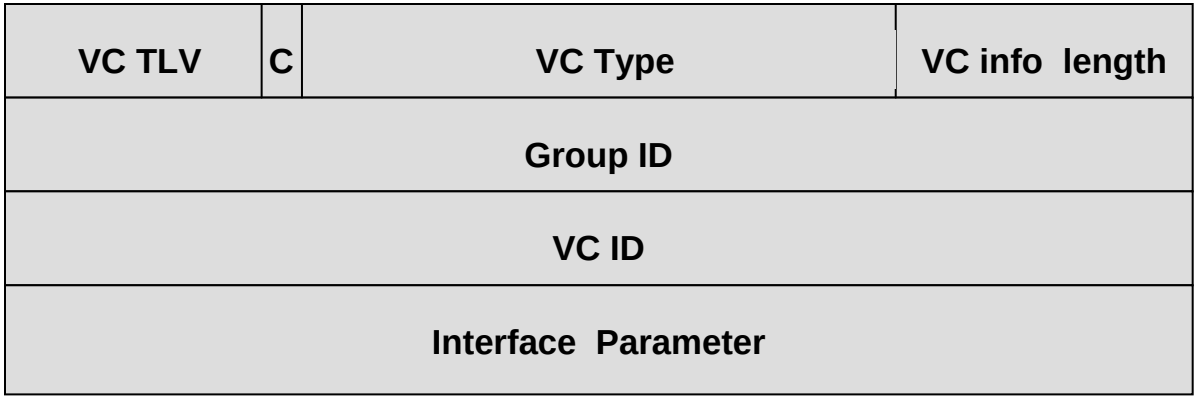
AToM: VC Label distributed through directed LDP session



PWid FEC TLV

CEM = SAToP E1, T1, E3, T3,
CESoPSN basic, CESoPSN TDM with CAS,
TDMoIP AAL1, TDMoIP AAL2

LDP: PWid FEC TLV



VC TLV = 128 or 0x80

VC Type:	0x0011	E1 (SaToP)
	0x0012	T1 (SaToP)
	0x0013	E3 (SaToP)
	0x0014	T3 (SaToP)
	0x0015	CESoPSN basic mode
	0x0017	CESoPSN TDM with CAS

C: 1 control word present

Group ID: If for a group of VC, useful to withdraws many labels at once

VC ID : ID for the transported L2 vc

Int. Param: classical + IETF-PWE3-TDM-CP-Extension

3 sub-TLV in latest [PWE3-CP] draft

- Sub-TLV's

  - Status sub-TLV: Goal is to map L2signaling status (LMI, AOM's) with this new TLV instead of mapping it with PW-TLV

    - Status TLV will indicate if PW is up/down

    - PW TLV will indicate if PW exist or not

  - Group sub-TLV: Same as group ID used in PWid FEC TLV.

  - Interfaces MTU sub-TLV: Inform on interface MTU, number of cells allow to be packed into alone MPLS frames.

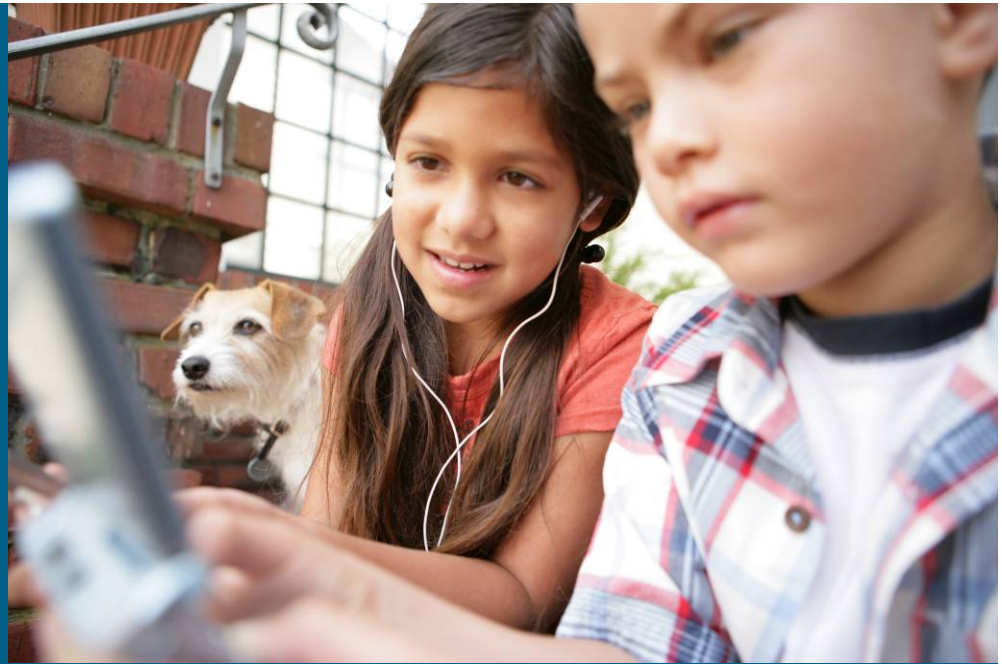
Few more sub-TLV defined in [PWE3-VCCV], [PWE3-fragmentation], [PWE3-segment]

New TDM sub-TLVs [PWE3-TDM-CP] draft

TDM sub-TLV (0x0B): Goal is to

- Indicate type of clocking mechanism utilized
- Indicate usage of RTP Header and parameters
- Indicate usage of CAS and formats.

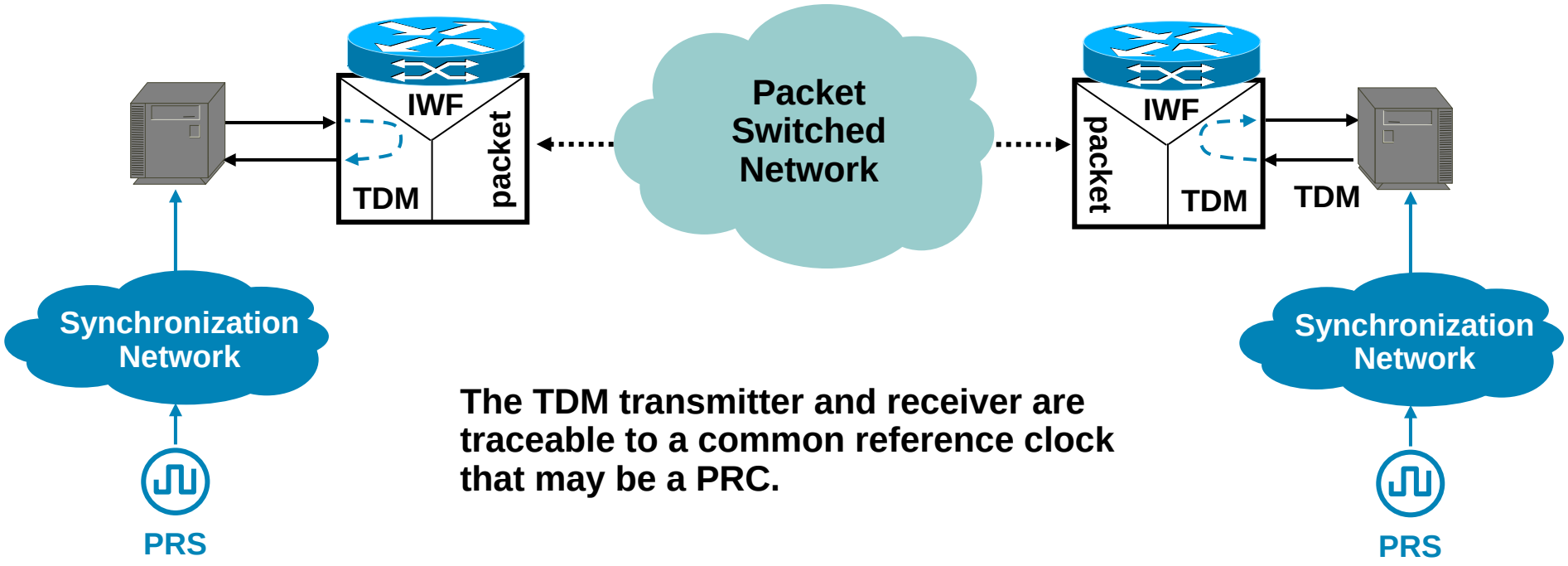
Circuit Emulation
Clocking



Clocking

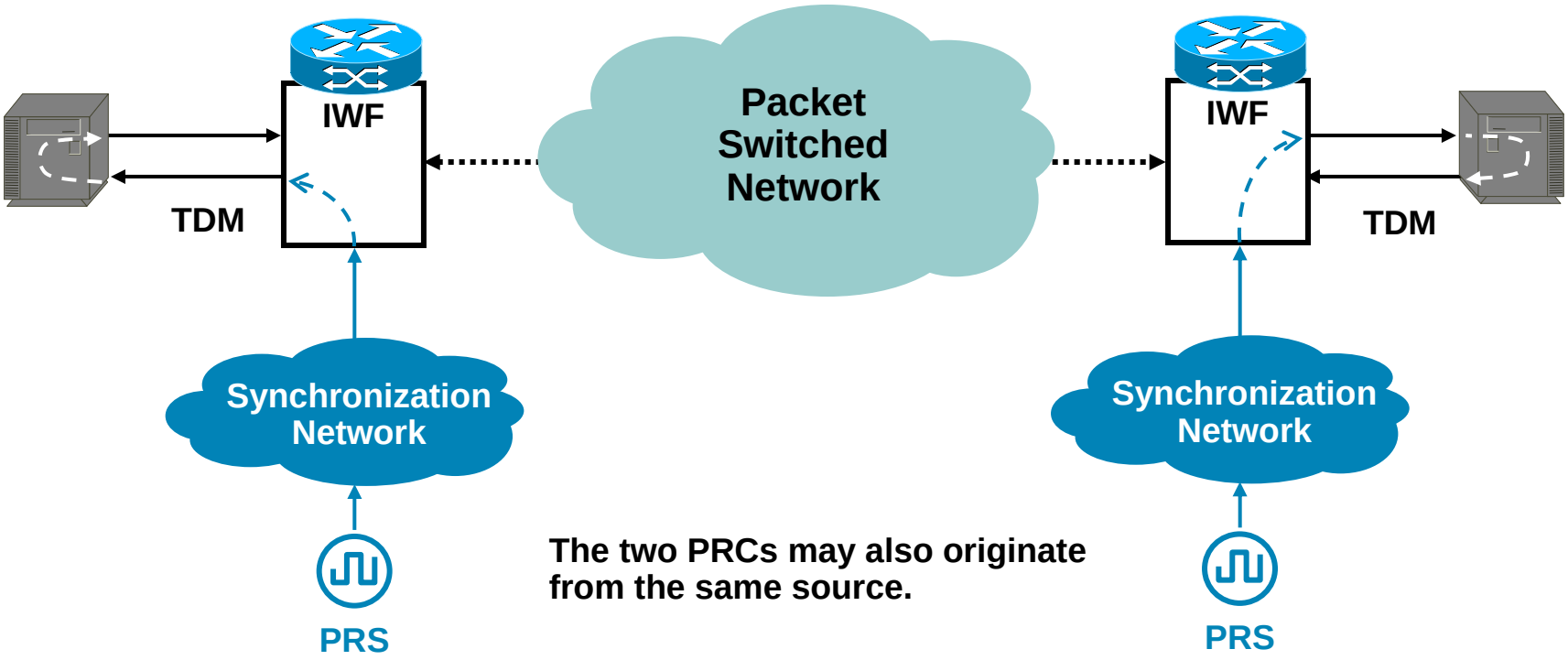
- Clock scenarios are outlined in RFC4197 Requirements for Edge-to-Edge Emulation of Time Division Multiplexed (TDM) Circuits over Packet Switching Networks
- On the wire, TDM PW encapsulation is standard; clock recovery algorithms at the receiving end are not defined (i.e. they are proprietary)
- Clocking is a major discipline in its own right

Network Synchronous operation
Reference clock at End Systems



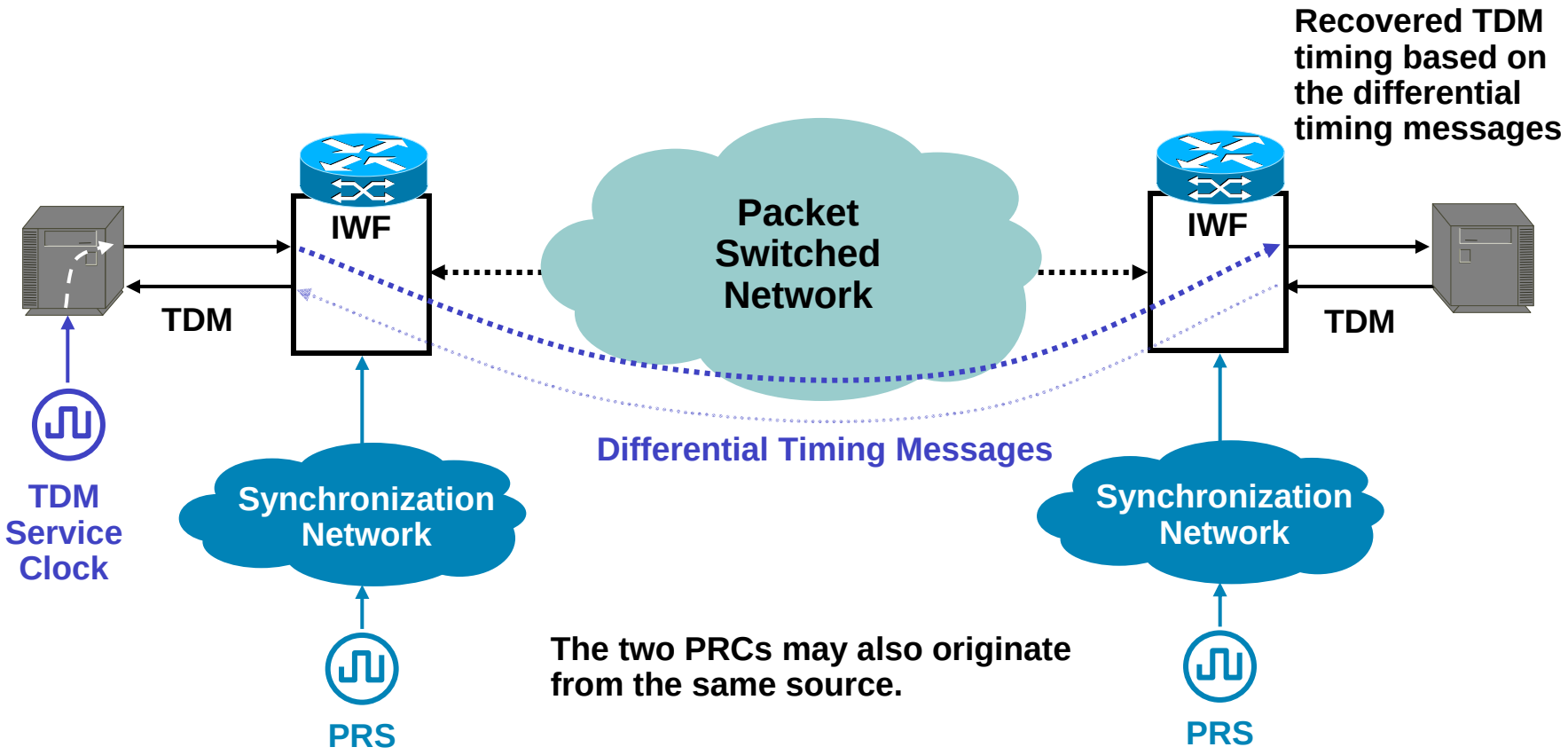
The TDM transmitter and receiver are traceable to a common reference clock that may be a PRC.

Network Synchronous Operation
Reference clock at IWF devices

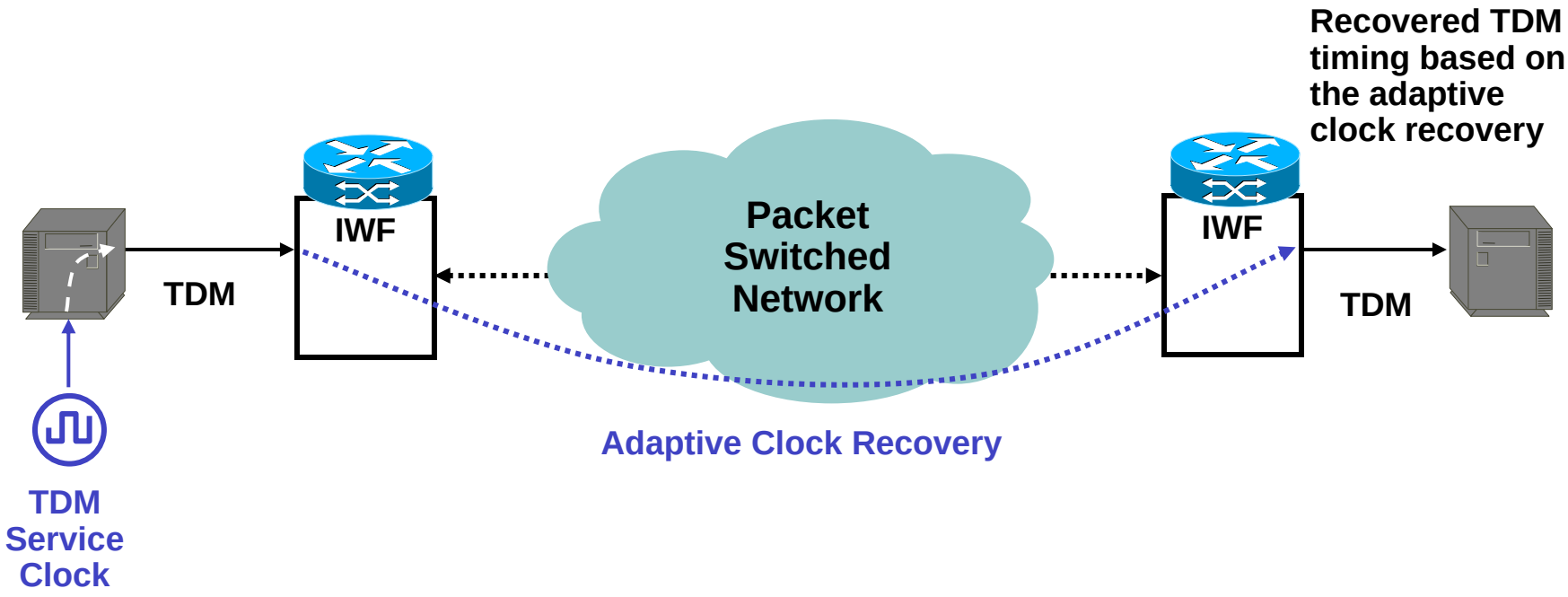


The two PRCs may also originate from the same source.

Timing Recovery based on the Differential Method

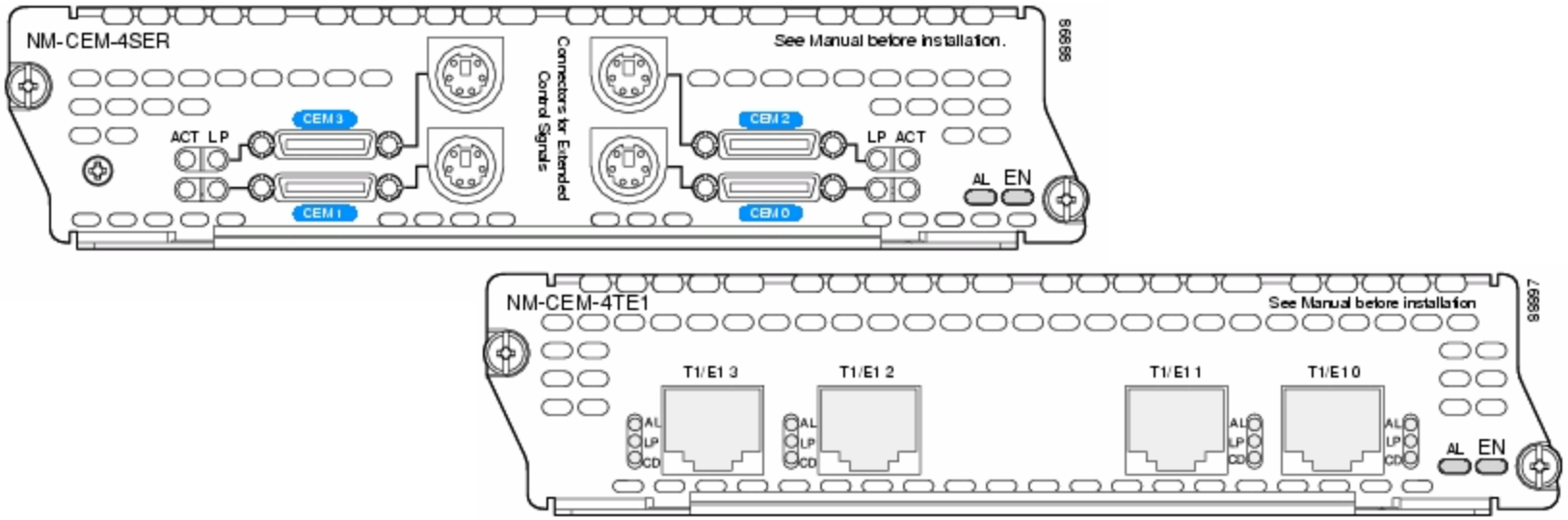


Timing Recovery based on the Adaptive Method



Circuit Emulation
Hardware

CEM-NM-4SER & CEM-NM-4TE1



- Interfaces: 4 Serial, E1/T1
- Circuit Emulation method: CE over IP / UDP
- Clocking method: Internal, loopback or adaptive.

Future

?

Circuit Emulation
Standard

ITU-T Specifications

[G.702] Digital Hierarchy Bit Rates

[G.704] Synchronous frame structure (FAS: Frame Alignment Signal)

[G.706] Frame Alignment and Cyclic Redundancy Check (OOF, CRC: Out of Frame Synchronization).

[G.775] LOS, AIS, RDI (RAI) definition: Loss of signal, Alarm Indication Signal, Remote Defect (Alarm) Indication.

[G.826] Error performance parameters and objectives for international, constant bit rate digital path at or above the primary rate.

[T1.107-1988] ANSI specifications.

IETF drafts

- RFC 3985 (PWE3 Architecture)
- RFC 4197 (PWE3 TDM Requirements)
- draft-ietf-pwe3-satop
- draft-ietf-pwe3-cesopsn
- draft-ietf-pwe3-tdmoip
- draft-ietf-pwe3-tdm-control-protocol-extensi
- draft-ieft-l2tpext-tdm

- draft-ietf-pwe3-sonet

Other Standards

- ITU - Y.1413 - TDM-MPLS network interworking - User plane interworking
- ITU – Y.1543 TDM – IP Interworking – User plane interworking
- ITU - G.8261 Timing and Synchronization aspects in Packet Networks (including over Ethernet).
- MEF 8 - Implementation Agreement for the Emulation of PDH Circuits over Metro Ethernet
- TDM Transport over MPLS using AAL1 Implementation Agreement (MPLS Forum)
- Emulation of TDM Circuits over MPLS Using Raw Encapsulation Implementation Agreement (MPLS Forum)

Meet the Experts
IP NGN Architectures and Technologies

- Oliver Boehmer
  Network Consulting Engineer

- Moustafa Kattan
  Consulting Systems Engineer

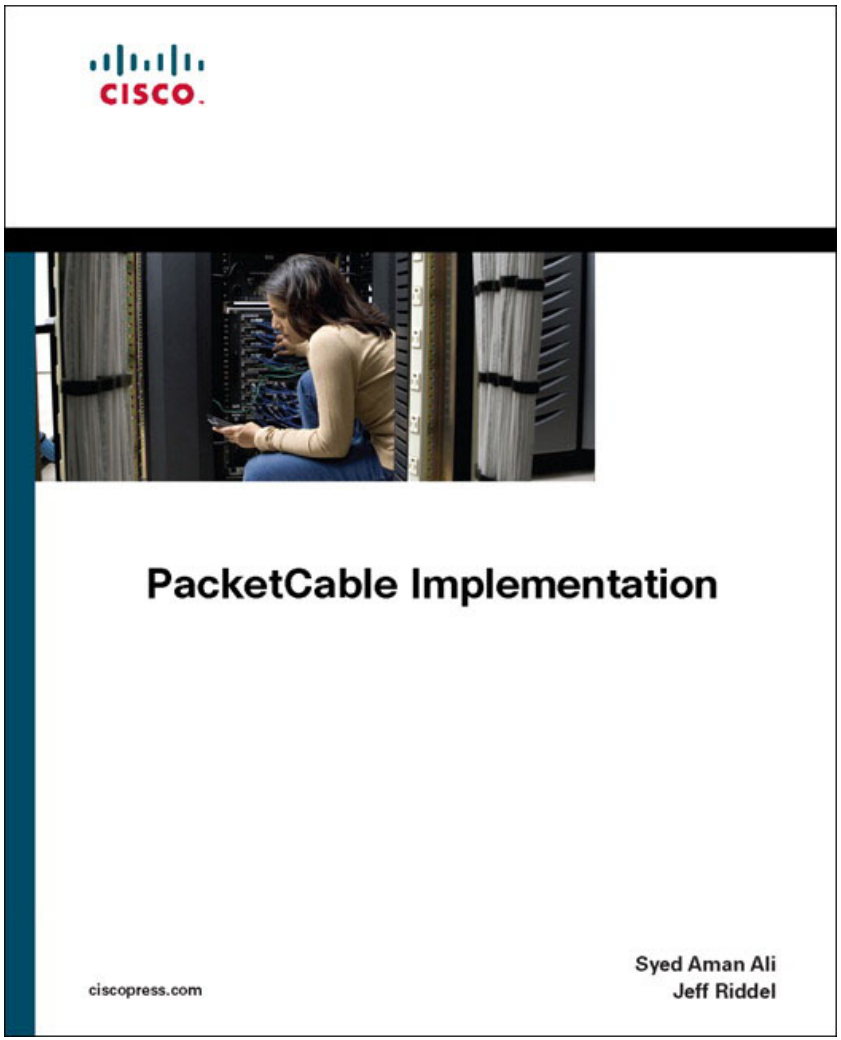
- Yves Hertoghs
  Distinguished System Engineer

- Ed Draiss
  Product Manager

Recommended Reading

BRKBBA -3012

- PacketCable Implementation (Feb 07)



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